APPENDIX A

To illustrate the concept of the present invention it is first useful to show a conventional motherboard/daughterboard mounting configuration. Referring to Figure 1, there is shown such a conventional motherboard/daughterboard mounting configuration 10, wherein a plurality of daughterboards 12 are shown mounted to a single motherboard 14. Each daughterboard 12 has electronic components 16 mounted thereon which are electrically connected to each other by signal conductors 18 in both the daughterboards 12 and the motherboard 14. The signal conductors 18 in the daughterboards 12 and the motherboard 14 are electrically connected via pin-and-box connectors 17. That is, electrically conductive contact pads 22 on the daughterboards 12 are placed into electrical contact with electrically conductive pins 19 within the pin-and-box connectors 17 (see Figure 1a). The electrically conductive pins 19 are electrically connected to electrically conductive contact pads or vias (not shown) on the motherboard 14. The electrically conductive contact pads 22 on the daughterboards 12 and the electrically conductive contact pads or vias on the motherboard 14 are in electrical connection with the signal conductors 18 in the daughterboards 12 and the motherboard 14, respectively. The pin-and-box connectors 1[9]7 are typically

constructed such that the daughterboards 12 are oriented at 90° with respect to the motherboard 14[, as r].

Referring to Figures 2A and 2B, a printed wiring board (PWB) includes a dielectric material 21 with a copper ground plane 25 coating a lower surface 2[5]3 of the PWB 11. In this embedded microstrip configuration, single-ended copper conductors 26 and 27, are embedded in a plane in the dielectric material 21 and extend parallel to each other and to an upper 24 and a lower 23 surface of the PWB. A V-shaped groove 29, running parallel to the copper conductors 26, 27, is provided on both sides of each conductor 26, 27 and extends from the upper surface 24 all the way to the lower ground plane 25. Only one complete groove 29 is illustrated, namely the one between conductors 26 and 27. The grooves 29 extend along the entire length of the copper conductors and are located equidistantly between the individual traces. The upper surface 24 of the PWB 11 is provided with a copper coating 28 which extends along the surfaces of the grooves 29 and into contact with the ground plane 25. Together with the ground plane 25, the copper coating 28 forms a complete shield around each signal conductor 26, 27. Via-in-pads 20 for connecting the conductors 26, 27 [to the upper surface 24 of the PWB 11] are also shown for completeness.

APPENDIX B

A1

To illustrate the concept of the present invention it is first useful to show a conventional motherboard/daughterboard mounting configuration. Referring to Figure 1, there is shown such a conventional motherboard/daughterboard mounting configuration 10, wherein a plurality of daughterboards 12 are shown mounted to a single motherboard 14. Each daughterboard 12 has electronic components 16 mounted thereon which are electrically connected to each other by signal conductors 18 in both the daughterboards 12 and the motherboard 14. The signal conductors 18 in the daughterboards 12 and the motherboard 14 are electrically connected via pin-and-box connectors 17. That is, electrically conductive contact pads 22 on the daughterboards 12 are placed into electrical contact with electrically conductive pins 19 within the pin-and-box connectors 17 (see Figure 1a). The electrically conductive pins 19 are electrically connected to electrically conductive contact pads or vias (not shown) on the motherboard 14. The electrically conductive contact pads 22 on the daughterboards 12 and the electrically conductive contact pads or vias on the motherboard 14 are in electrical connection with the signal conductors 18 in the daughterboards 12 and the motherboard 14, respectively. The pin-and-box connectors 17 are typically

A1 Cont

constructed such that the daughterboards 12 are oriented at 90° with respect to the motherboard 14.

Referring to Figures 2A and 2B, a printed wiring board (PWB) includes a dielectric material 21 with a copper ground plane 25 coating a lower surface 23 of the PWB 11. In this embedded microstrip configuration, single-ended copper conductors 26 and 27, are embedded in a plane in the dielectric material 21 and extend parallel to each other and to an upper 24 and a lower 23 surface of the PWB. A V-shaped groove 29, running parallel to the copper conductors 26, 27, is provided on both sides of each conductor 26, 27 and extends from the upper surface 24 all the way to the lower ground plane 25. Only one complete groove 29 is illustrated, namely the one between conductors 26 and 27. The grooves 29 extend along the entire length of the copper conductors and are located equidistantly between the individual traces. The upper surface 24 of the PWB 11 is provided with a copper coating 28 which extends along the surfaces of the grooves 29 and into contact with the ground plane 25. Together with the ground plane 25, the copper coating 28 forms a complete shield around each signal conductor 26, 27. Via-in-pads 20 for connecting the conductors 26, 27 are also shown for completeness.

APPENDIX C

13 (Amended). A system for electrically interconnecting [a signal between] circuit boards, the system comprising:

a first circuit board having a first signal conducting means formed therein, the first signal conducting means being shielded by a first electrically conductive shield, the first electrically conductive shield having a first opening formed therein so as to expose the first signal conducting means in the first circuit board;

a second circuit board having a second signal conducting means formed therein, the second signal conducting means being shielded by a second electrically conductive shield, the second electrically conductive shield having a second opening formed therein so as to expose the second signal conducting means in the second circuit board; and

an electrically conductive [adhesive, solder paste, or interposer/elastomer device applied] material surrounding at least one of [thee] the first and second openings and within at least one of the first and second openings;

wherein the first circuit board and the second circuit board are electrically interconnected by the electrically conductive [adhesive, solder paste, or interposer/elastomer device] material such that the first opening and the second

opening are aligned and [a signal propagating along] the first signal conducting means is electrically interconnected to the second signal conducting means.

14 (Amended). The system as defined in claim 13, [further comprising:] wherein the electrically conductive material comprises an electrically conductive adhesive, [or] solder paste, or interposer/elastomer device disposed within a first via located within the first opening and within a second via located within the second opening.

19 (Amended). The system as defined in claim 1[3]8, wherein the first signal conductor and the second signal conductor are formed on respective signal layers of the first circuit board and the second circuit board, wherein the signal layers are disposed beneath the ground plane layers in the first circuit board and the second circuit board.

20 (Amended). The system as defined in claim 13, wherein [the signal is] a high speed signal carrying data at a rate on the order of 1 Gb/s and above propagates from the first signal conductor to the second signal conductor via the electrically conductive material.

21 (Amended). The system as defined in claim 13,

wherein the first circuit board has a third signal conducting means formed therein, wherein the third signal conducting means is shielded by a third electrically conductive shield, wherein a third opening is formed in the third electrically conductive shield so as to expose the third signal conducting means in the first circuit board;

wherein the second circuit board has a fourth signal conducting means formed therein, wherein the fourth signal conducting means is shielded by a fourth electrically conductive shield, wherein a fourth opening is formed in the fourth electrically conductive shield so as to expose the fourth signal conducting means in the second circuit board;

wherein an electrically conductive [adhesive, solder paste, or interposer/elastomer device] material is applied around at least one of the third and fourth openings and within at least one of the third and fourth openings; and

wherein the first circuit board and the second circuit board are positioned such that the third opening and the fourth opening are aligned and [a another signal propagating along] the third signal conducting means is electrically connected to the fourth signal conducting means.

24 (Amended). The system as defined in claim 2[2]3, wherein the daughterboard is formed at least partially of flexible material so as to allow angular mating with the motherboard.

28 (Amended). A system for electrically interconnecting [a signal between] circuit boards, the system comprising:

a first circuit board having a first signal conducting means formed therein, the first signal conducting means being shielded by a first electrically conductive shield, the first electrically conductive shield having a first opening formed therein so as to expose the first signal conducting means in the first circuit board; and

a second circuit board having a second signal conducting means formed therein; and

an electrically conductive [adhesive, solder paste, or interposer/elastomer device] material surrounding the first opening and applied within the first opening,

wherein the first circuit board and the second circuit board are positioned such that the first signal conducting means and the second signal conducting means are aligned through the opening and [a signal propagating along] the first signal conducting means is electrically interconnected to the second

signal conducting means.

APPENDIX D

12

13 (Amended). A system for electrically interconnecting circuit boards, the system comprising:

a first circuit board having a first signal conducting means formed therein, the first signal conducting means being shielded by a first electrically conductive shield, the first electrically conductive shield having a first opening formed therein so as to expose the first signal conducting means in the first circuit board;

a second circuit board having a second signal conducting means formed therein, the second signal conducting means being shielded by a second electrically conductive shield, the second electrically conductive shield having a second opening formed therein so as to expose the second signal conducting means in the second circuit board; and

an electrically conductive material surrounding at least one of the first and second openings and within at least one of the first and second openings;

wherein the first circuit board and the second circuit board are electrically interconnected by the electrically conductive material such that the first opening and the second opening are aligned and the first signal conducting means is electrically interconnected to the second signal conducting

means.

A2 Cont

14 (Amended). The system as defined in claim 13, wherein the electrically conductive material comprises an electrically conductive adhesive, solder paste, or interposer/elastomer device disposed within a first via located within the first opening and within a second via located within the second opening.

15. The system as defined in claim 13, wherein the first signal conducting means comprises a pair of signal conductors and the second signal conducting means comprises a pair of signal conductors.

16. The system as defined in claim 15, wherein the first signal conducting means and the second signal conducting means each comprise a single conductor.

17. The system as defined in claim 13, wherein the first circuit board and the second circuit board are multilayer circuit boards, wherein the first electrically conductive shield and the second electrically conductive shield are respective electrically conductive layers of the first circuit board and

the second circuit board.

18. The system as defined in claim 13, wherein the first electrically conductive shield and the second electrically conductive shield are formed by respective ground plane layers of the first circuit board and the second circuit board.

A2 Cont

19 (Amended). The system as defined in claim 18, wherein the first signal conductor and the second signal conductor are formed on respective signal layers of the first circuit board and the second circuit board, wherein the signal layers are disposed beneath the ground plane layers in the first circuit board and the second circuit board.

20 (Amended). The system as defined in claim 13, wherein a high speed signal carrying data at a rate on the order of 1 Gb/s and above propagates from the first signal conductor to the second signal conductor via the electrically conductive material.

21 (Amended). The system as defined in claim 13,

wherein the first circuit board has a third signal conducting means formed therein, wherein the third signal conducting means is shielded by a third electrically conductive

shield, wherein a third opening is formed in the third electrically conductive shield so as to expose the third signal conducting means in the first circuit board;

A2 Cont

wherein the second circuit board has a fourth signal conducting means formed therein, wherein the fourth signal conducting means is shielded by a fourth electrically conductive shield, wherein a fourth opening is formed in the fourth electrically conductive shield so as to expose the fourth signal conducting means in the second circuit board;

wherein an electrically conductive material is applied around at least one of the third and fourth openings and within at least one of the third and fourth openings; and

wherein the first circuit board and the second circuit board are positioned such that the third opening and the fourth opening are aligned and the third signal conducting means is electrically connected to the fourth signal conducting means.

22. The system as defined in claim 21, wherein the third electrically conductive shield is electrically connected to the first electrically conductive shield, wherein the fourth electrically conductive shield is electrically connected to the second electrically conductive shield.

23. The system as defined in claim 13, wherein the first circuit board is a motherboard, wherein the second circuit board is a daughterboard.

A2 Cont

24 (Amended). The system as defined in claim 23, wherein the daughterboard is formed at least partially of flexible material so as to allow angular mating with the motherboard.

A3

28 (Amended). A system for electrically interconnecting circuit boards, the system comprising:

a first circuit board having a first signal conducting means formed therein, the first signal conducting means being shielded by a first electrically conductive shield, the first electrically conductive shield having a first opening formed therein so as to expose the first signal conducting means in the first circuit board; and

a second circuit board having a second signal conducting means formed therein; and

an electrically conductive material surrounding the first opening and applied within the first opening,

wherein the first circuit board and the second circuit board are positioned such that the first signal conducting means and the second signal conducting means are aligned through the

opening and the first signal conducting means is electrically interconnected to the second signal conducting means.

29. The system as defined in claim 28, wherein the first signal conducting means comprises a first pair of conductors and the second signal conducting means comprises a second pair of conductors and each conductor of the first pair is connected with a conductor of the second pair for transmission of two signals between the first pair and the second pair.

30. The system as defined in claim 28, wherein the first signal conducting means comprises a single conductor and the second signal conducting means comprises a single conductor.